Applicant: Shigeharu Monoe Attorney's Docket No.: 12732-158001 / US6490

Serial No.: 10/603,944 Filed: June 26, 2003

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Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1. (Currently amended) A manufacturing method of a semiconductor device comprising:

forming a laminate structure comprising a lower first conductive layer and an upper second conductive layer over a semiconductor layer with a gate insulating film interposed therebetween between the semiconductor layer and the conductive layers;

forming a mask pattern over the laminate structure;

forming a first conductive layer pattern having a tapered edge by etching the second conductive layer and the first conductive layer;

recessing an edge of the mask pattern remaining on the first conductive layer pattern;

after recessing the edge of the mask pattern, forming a second conductive layer pattern
by selectively etching the second conductive layer in the first conductive layer pattern in
accordance with [[of]] the mask pattern; and

forming an LDD region in a region of the semiconductor layer overlapping with the first conductive layer in the second conductive layer pattern by using the second conductive layer in the second conductive layer pattern as a mask for shielding ions accelerated by an electric field.

- 2. (Original) The method according to claim 1, wherein the first conductive layer is made of tungsten, and the second conductive layer is made of aluminum or metal having aluminum as the main component.
- 3. (Original) The method according to claim 1, wherein the edge of the mask pattern remaining on the first conductive layer pattern is recessed by oxygen plasma treatment.

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4. (Currently amended) A manufacturing method of a semiconductor device comprising:

forming a laminate structure over a semiconductor layer by sequentially depositing a first conductive layer, a second conductive layer, and a third conductive layer with a gate insulating film interposed therebetween between the semiconductor layer and the conductive layers;

forming a mask pattern on the laminate structure;

forming a first conductive layer pattern having a tapered edge;

recessing an edge of the mask pattern remaining on the first conductive layer pattern;

after recessing the edge of the mask pattern, forming a second conductive layer pattern by selectively etching the third conductive layer and the second conductive layer in the first conductive layer pattern on the in accordance with basis of the mask pattern; and

forming an LDD region in a region of the semiconductor layer overlapping with the first conductive layer in the second conductive layer pattern by using the third conductive layer and the second conductive layer in the second conductive layer pattern as a mask for shielding ions accelerated by an electric field.

- 5. (Original) The method according to claim 4, wherein the first conductive layer is made of tungsten, the second conductive layer is made of aluminum or alloy or compound having aluminum as the main component, and the third conductive layer is made of titanium nitride.
- 6. (Original) The method according to claim 4, wherein the edge of the mask pattern remaining on the first conductive layer pattern is recessed by oxygen plasma treatment.
- 7. (Currently amended) A manufacturing method of a semiconductor device comprising:

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forming a laminate structure comprising a lower first conductive layer and an upper second conductive layer over a semiconductor layer with a gate insulating film interposed therebetween between the semiconductor layer and the conductive layers;

forming a mask pattern on the laminate structure;

performing plasma treatment for decreasing the taper angle of an edge of the mask pattern;

after performing plasma treatment, forming a first conductive layer pattern having a tapered edge by etching the second conductive layer and the first conductive layer of the laminate structure by using the mask pattern;

forming a second conductive layer pattern by selectively etching the second and third conductive layers in the first conductive layer pattern; and

forming an LDD region in a region of the semiconductor layer overlapping with the first conductive layer in the second conductive layer pattern by using the second conductive layer in the second conductive layer pattern as a mask for shielding ions accelerated by an electric field.

- 8. (Original) The method according to claim 7, wherein the first conductive layer is made of tungsten, and the second conductive layer is made of aluminum or metal having aluminum as the main component.
- 9. (Original) The method according to claim 7, wherein the edge of the mask pattern remaining on the first conductive layer pattern is recessed by oxygen plasma treatment.
- 10. (Original) The method according to claim 7, wherein the width of the mask pattern is decreased by plasma treatment using a fluorine-based gas.
- 11. (Currently amended) A manufacturing method of a semiconductor device comprising:

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forming a laminate structure over a semiconductor layer by sequentially depositing a first conductive layer, a second conductive layer, and a third conductive layer with a gate insulating film interposed therebetween between the semiconductor layer and the conductive layers;

forming a mask pattern on the laminate structure;

performing plasma treatment for etching the third conductive layer and decreasing the taper angle of an edge of the mask pattern;

after performing plasma treatment, forming a first conductive layer pattern having a tapered edge by etching the second conductive layer and the first conductive layer of the laminate structure by using the mask pattern;

forming a second conductive layer pattern by selectively etching the second and third conductive layers in the first conductive layer pattern; and

forming an LDD region in a region of the semiconductor layer overlapping with the first conductive layer in the second conductive layer pattern by using the second and third conductive layers in the second conductive layer pattern as a mask for shielding ions accelerated by an electric field.

- 12. (Original) The method according to claim 11, wherein the edge of the mask pattern remaining on the first conductive layer pattern is recessed by oxygen plasma treatment.
- 13. (Original) The method according to claim 11, wherein the width of the mask pattern is decreased by plasma treatment using a fluorine-based gas.